II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microelectronic device, comprising:

~~a first semiconductor substrate bonded to a second semiconductor substrate, the first semiconductor substrate including an opening through which an epitaxially grown portion of the second semiconductor substrate extends~~

a discrete first wafer bonded to a discrete second wafer, wherein:

the first wafer comprises a first semiconductor substrate, the second wafer comprises a second semiconductor substrate, and the discrete first and second wafers are bonded such that the first semiconductor substrate and the second semiconductor substrate are proximate the bond between the discrete first and second wafers;

one of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation; and

an epitaxially grown portion of the second semiconductor substrate extends through an opening in the first wafer, including through the first semiconductor substrate;

a shallow trench isolation interposing a sidewall of the opening and the epitaxially grown portion of the second semiconductor substrate, wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate, and extends into the second semiconductor substrate;

a first semiconductor device coupled to the first semiconductor substrate; and

a second semiconductor device coupled to the epitaxially grown portion of the second semiconductor substrate.

2. (Currently Amended) The device of claim 1 wherein one of the first and second semiconductor ~~device~~ devices comprises a p-type transistor and the other of the first and second semiconductor ~~device~~ devices comprises an n-type transistor.

3. (Cancelled).

4. (Cancelled).

5. (Currently Amended) The device of claim 1 wherein the first semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation.

6. (Currently Amended) The device of claim 1 wherein the first semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation.

7. (Cancelled).

8. (Cancelled).

9. (Currently Amended) The device of claim 1 further comprising an oxide layer interposing the first semiconductor substrate and ~~a bulk portion of~~ the second ~~semiconductor substrate~~ wafer, the opening also extending through the oxide layer.

10. (Currently Amended) The device of claim 1 further comprising a silicon dioxide layer interposing the first semiconductor substrate and ~~a bulk portion of~~ the second ~~semiconductor substrate~~ wafer, the opening also extending through the silicon dioxide layer.

11. (Currently Amended) The device of claim 1 further comprising an implanted oxide layer interposing the first semiconductor substrate and ~~a bulk portion of~~ the second ~~semiconductor substrate~~ wafer, the opening also extending through the implanted oxide layer.

12. (Original) The device of claim 1 wherein the first semiconductor substrate is a silicon-on-insulator substrate.

13. (Currently Amended) A method of manufacturing a microelectronic device, comprising:

~~coupling a first semiconductor substrate to a second semiconductor substrate~~

coupling a discrete first wafer having a first semiconductor substrate to a discrete second wafer having a second semiconductor substrate such that the first and second semiconductor substrates are proximate the second and first wafers, respectively, wherein one of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation;

forming a shallow trench isolation spanning the thickness of the first wafer, including the first semiconductor substrate, and extending into the second semiconductor substrate;

patterning an opening in the first wafer, including through the first semiconductor substrate, and adjacent the shallow trench isolation;

growing epitaxially an extension of the second semiconductor substrate through the opening and adjacent the shallow trench isolation, such that the epitaxially grown extension of the second semiconductor substrate is laterally isolated from the first semiconductor substrate by the shallow trench isolation;

forming a first semiconductor device on the first semiconductor substrate; and

forming a second semiconductor device on the extension of the second semiconductor substrate.

14. (Currently Amended) The method of claim 13 wherein one of the first and second semiconductor ~~device~~ devices comprises a p-type transistor and the other of the first and second semiconductor ~~device~~ devices comprises an n-type transistor.

15. (Cancelled).

16. (Cancelled).

17. (Currently Amended) The method of claim 13 wherein the first semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation.

18. (Currently Amended) The method of claim 13 wherein the first semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation.

19. (Currently Amended) The method of claim 13 further comprising forming a dielectric film on the first ~~semiconductor substrate~~ wafer opposite the second semiconductor substrate ~~and one at least a portion of a surface of the opening~~ before epitaxially growing the extension of the second semiconductor substrate.

20. (Currently Amended) The method of claim 19 further comprising planarizing the first ~~semiconductor substrate~~ wafer, the dielectric film, and the extension of the second semiconductor substrate to form a substantially planar surface collectively therefrom.

21. (Original) The method of claim 20 wherein planarizing includes substantially removing all of the dielectric film not located in the opening.

22. (Cancelled).

23. (Currently Amended) The method of claim 13 further comprising forming an oxide layer on a surface of one of the first and second wafers proximate an interface between the first semiconductor substrate and the second semiconductor substrate prior to ~~forming the opening~~ coupling the first and second wafers, the opening also extending through the oxide layer.

24. (Cancelled).

25. (Currently Amended) The method of claim 13 wherein coupling the first ~~semiconductor substrate to the second semiconductor substrate~~ and second wafers includes bonding the first ~~semiconductor substrate to the second semiconductor substrate~~ and second wafers.

26. (Currently Amended) The method of claim 25 wherein ~~the first and second semiconductor substrates comprise first and second wafers, respectively, and wherein~~ bonding comprises wafer bonding.

27. (Currently Amended) An integrated circuit device, comprising:

~~a discrete first wafer including a first semiconductor substrate having a plurality of openings extending therethrough;~~

~~a discrete second wafer including a second semiconductor substrate coupled to the first semiconductor substrate and including a plurality of epitaxially grown extensions each extending through a corresponding one of the plurality of openings;~~

a discrete first wafer including a first semiconductor substrate, wherein a plurality of openings extends through the first wafer, including through the first semiconductor substrate;

a discrete second wafer coupled to the first wafer, wherein the second wafer includes a second semiconductor substrate and a plurality of extensions grown epitaxially from the second semiconductor substrate and extending through corresponding ones of the plurality openings in the first wafer, and wherein one of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation;

a plurality of shallow trench isolation structures each interposing a sidewall of one of the plurality of openings and a corresponding one of the plurality of extensions of the second semiconductor substrate, wherein each of the plurality of shallow trench isolation structures spans the thickness of the first wafer, including the thickness of the first semiconductor substrate, and extends at least partially into the second semiconductor substrate;

a plurality of first semiconductor devices each coupled to the first semiconductor substrate; and

a plurality of second semiconductor devices each coupled to a corresponding one of the plurality of extensions.

28. (Original) The integrated circuit device of claim 27 wherein ones of the plurality of first semiconductor devices each comprise a p-type transistor and ones of the plurality of second semiconductor devices each comprise an n-type transistor.

29. (Original) The integrated circuit device of claim 27 wherein ones of the plurality of first semiconductor devices each comprise an n-type transistor and ones of the plurality of second semiconductor devices each comprise a p-type transistor.

30. (Cancelled).

31. (Currently Amended) The integrated circuit device of claim 27 wherein the first semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation.

32. (Currently Amended) The integrated circuit device of claim 27 wherein the first semiconductor substrate has [[a]] the (1,0,0) crystallographic orientation and the second semiconductor substrate has [[a]] the (1,1,0) crystallographic orientation.

33. (Cancelled).

34. (Cancelled).

35. (Currently Amended) The integrated circuit device of claim 27 further comprising an oxide layer interposing the first ~~semiconductor substrate~~ and ~~a bulk portion of the~~ second ~~semiconductor substrate~~ wafers, the plurality of openings each also extending through the oxide layer.

36. (Original) The integrated circuit device of claim 35 wherein the oxide layer comprises silicon dioxide.

37. (Original) The integrated circuit device of claim 35 wherein the oxide layer comprises an implanted oxide layer.

38. (Original) The integrated circuit device of claim 27 wherein at least one of the first and second semiconductor substrates is a silicon-on-insulator substrate.